



## ACM Transactions on Embedded Computing

Call for papers

### Special Issue on **Secure and Fault-tolerant Embedded Computing**

#### **About this Special Issue**

With technology scaling to unprecedented levels, electronic systems design in general and embedded system design in particular, is increasingly becoming more challenging. This is mainly due to shorter time-to-market demands with strict design constraints related to power, performance, and reliability. In recent years, security and fault tolerance have become important design goals, especially in the face of powerful implementation-specific threats such as Hardware Trojan Horses and Fault Injection Attacks. Meeting these design goals, while at the same time ensuring security and fault tolerance, has become extremely challenging because of difficulty in comprehensive verification of complex implementations at the current state-of-the-art, and since many of these threats arise dynamically during runtime. Hence, embedded systems must be designed and implemented in a fault-tolerant manner to meet reliability goals, especially for critical cyber-physical applications such as bio-medical appliances. The extreme resource constraint common in many embedded systems add extra challenges in adopting traditional fault-tolerant techniques.

This special issue will be dedicated to research and advances on the issues in Secure and Fault-tolerant Embedded Computing. Original papers describing new and previously unpublished works will be selected addressing all aspects of security and fault tolerance in embedded computing, covering both hardware and software fault tolerance, and possibly hardware-software co-design approaches. The papers will go through the usual review process, and then further reviewed by the editorial team to ensure quality of publication.

The topics of interest in this special issue include, but are not limited to:

- **Vulnerability estimation and mitigation techniques against fault attacks in embedded systems**
- **Fault injection attacks and other attacks targeting embedded systems**
- **Novel Hardware Trojan Horse design in IPs and embedded devices**

- **Hardware Trojan Horse detection and mitigation approaches, including Design for Testability (DFT) techniques**
- **Effective approaches for fault tolerance of cyber-physical systems, with emphasis on low-overhead techniques**
- **Runtime support for fault tolerance in multi-core architectures**
- **Hardware-software co-design approaches for security and fault tolerance**
- **Protection against counterfeiting of embedded systems, including through applications of Physically Unclonable Functions (PUFs)**
- **Fault attack injection, detection and protection**
- **Reconfigurable devices for security and fault tolerance**
- **Validation of secure and fault tolerance embedded systems**

The manuscript must not be under consideration for publication elsewhere. Conference papers may only be submitted if the paper was completely re-written or substantially extended (30%). Authors should submit their journal version at the ACM TECS Manuscript Central website (<https://mc.manuscriptcentral.com/tecs>) strictly adhering to the formatting instructions on the TECS website, and indicate that you are submitting to the Special Issue on **Secure and Fault-tolerant Embedded Computing** on the first page and in the field "Author's Cover Letter:" in Manuscript Central. The page count limit is 25. For additional questions please contact the guest editors.

### **Important Dates**

<b>Submission Deadline</b>	<b>1 June, 2016</b>
<b>Results of First Round of Reviews:</b>	<b>30 September, 2016</b>
<b>Submission of Revised Manuscripts</b>	<b>30 November, 2016</b>
<b>Results of Second Round of Reviews</b>	<b>30 December, 2016</b>
<b>Publication Materials Due</b>	<b>15 January, 2017</b>

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