

# **ACM TECS Special Issue on Virtual Prototyping of Parallel and Embedded Systems**

**Call for Papers  
Special Issue on**

## **Virtual Prototyping of Parallel and Embedded Systems - VIPES**

The Workshop on Virtual Prototyping of Parallel and Embedded Systems VIPES is an annual workshop and is sponsored by the IEEE Computer Society's Technical Committee on Parallel Processing.

This special issue of ACM Transactions on Embedded Computing Systems (ACM TECS) invites authors who presented their work at the VIPES workshop (2014-2015), as well as all researchers who work in the area of Virtual Prototyping.

Virtual prototyping stands for the development of hardware/software systems without using a real hardware prototype, i.e. no printed circuit board with electronic devices such as processors, field programmable gate arrays, peripherals and other devices is needed. The advantage is the possibility to exchange parts in the system setup with faster turnaround times in comparison with the traditional development process, where a time consuming redesign of the complete board has to be done. Since some years, the community exploiting these novel methods has grown as time to market plays a major role in industry. Additionally, the increasing complexity of embedded systems, which are more and more realized as parallel and distributed cyber-physical system, forces to perform a time-consuming design space exploration. For academics virtual prototyping is a hot topic and is used to develop future systems and to enable an outlook into the next generation of embedded systems and devices. The wide range of application scenarios for this type of development includes amongst others automotive, avionics, railway and medicine applications.

**This special issue targets the domain of virtual prototyping focusing the following topics**

- Virtual prototyping development tools
- Methods for virtual prototyping of complex systems
- Application development with virtual platforms
- Methods for Hardware / Software Codesign with virtual platforms
- Design space exploration for parallel and distributed multicore and cyber-physical systems
- Estimation of system characteristics in an early stage of development
- Functional verification at a high level of abstraction
- Methods for modeling of IP cores with SystemC
- Usage of Architecture Description Languages (ADL) for IP – core development

## Timetable

Submission due	<b>October 16th, 2015 (extended deadline)</b>
First Review results:	approx. end Nov, 2015
Final decision:	Feb. 29th, 2016

**Please notice that the scheduled review dates are approximate dates and subject to change. We will kindly inform you about the review results as soon as a decision was made. Questions regarding the disclosure of the review results should be addressed to the [guest editors](#).**

## Submission

Authors should submit their journal version at Manuscript Central adhering to the formatting instructions on the TECS Web page and indicate that the submission is meant to this special issue. To do so, add: "**Submitted to Special Issue on Virtual Prototyping of Parallel and Embedded Systems**" on the first page, in the field "**Author's Cover Letter**". Without indication, your submission cannot be considered for the special issue. For additional questions please send an email to the [guest editors](#).

**Page limit:** The page limit is fixed to 25 pages, additional pages will not be allowed.

- [Submission via Manuscript Central](#)
- [Author Information](#)
- [ACM TECS Web page](#)

## Guest Editors

- Jeronimo Castrillon, TU Dresden, Germany, [jeronimo.castrillon@tu-dresden.de](mailto:jeronimo.castrillon@tu-dresden.de)
- Cristina Silvano, Politecnico di Milano, Italy, [cristina.silvano@polimi.it](mailto:cristina.silvano@polimi.it)